Claims:

1. A semiconductor memory device comprising:

a substrate having electrical circuitry formed thereon;

a nanotube connected substantially orthogonal to the substrate;

a conductive ring about the exterior of the nanotube, the conductive ring providing electrical connection from the nanotube to the electrical circuitry on the substrate; and

wherein the nanotube forms a cell of a capacitor and a channel of a transistor.

2. The device of claim 1 wherein, the nanotube is a carbon nanotube.

3. A memory cell comprising:

a vertical transistor including a gate, source, drain, and channel wherein a nanotube forms the channel; and

a capacitor.

4. The device of claim 3 wherein, the nanotube is a carbon nanotube.

5. The device of claim 3 wherein, the nanotube forms a cell of the capacitor.

6. The device of claim 4 further including a capacitor ground cell plate formed on the nanotube.

7. A memory cell comprising:

a vertical transistor having about a 6 kohm connection resistance, the vertical transistor including a gate, source, drain, and channel, wherein a nanotube forms the channel; and

a capacitor, wherein the nanotube forms a cell of the capacitor.

8. A DRAM cell comprising:

a vertical transistor including a gate, source, drain, and channel wherein a nanotube forms the channel; and

a capacitor having a ground plate, an insulator, and a charge plate wherein the nanotube forms the charge plate.

9. The device of claim 8 wherein, the gate comprises a conductive ring about an insulated exterior section of the nanotube.

10. The device of claim 8 wherein, the source comprises a conductive ring about the exterior of the nanotube.

11. The device of claim 10 wherein, the source directly, physically contacts the nanotube.

12. The device of claim 8 wherein, the nanotube is substantially orthogonal to a substrate upon which the device is formed.

13. The device of claim 8 wherein, the nanotube is a carbon nanotube.

14. A vertical transistor in a memory cell device, the vertical transistor comprising:

a substrate;

a nanotube connected substantially orthogonal to the substrate;

a source and drain formed on the substrate;

a conductive ring formed about an insulated exterior section of the nanotube, the conductive ring forming the gate of the vertical transistor; and

wherein the nanotube forms a channel of the vertical transistor.

15. The device of claim 14 wherein, the memory cell device includes a capacitor having a capacitor cell formed by the nanotube and the nanotube is formed of carbon.

16. A memory cell capacitor comprising:

a substrate having a first surface defining a plane;

a nanotube connected substantially vertically to the substrate in relation the plane;

a ground cell plate formed on an exterior wall of the nanotube; and

wherein the nanotube forms a cell of the capacitor.

17. A semiconductor device comprising:

a substrate having a first surface;

an insulator formed on the first surface of the substrate;

a nanotube connected substantially perpendicular to the substrate;

alternating layers of insulative material, and conductive material formed about an exterior wall of the nanotube, wherein the conductive layers form gates for multiple transistors; and

wherein the nanotube forms an interconnection between the gates of the multiple transistors.

18. A semiconductor device having an electrical interconnect comprising:

a substrate having a first surface defining a plane;

a first trace formed on a portion of the substrate;

a nanotube having a first end connected to the first trace, the nanotube being substantially vertical in relation to the plane defined by the first surface of the substrate;

a second trace connected to a second end of the nanotube; and

wherein the nanotube forms an electrical connection between the first trace and the second trace.

19. The device of claim 18 wherein, the nanotube has about a 6 kohm resistance between the first trace and the second trace.

20. The device of claim 18 further comprising plural nanotubes.

21. A method of making a semiconductor device comprising:

providing a substrate;

forming a first insulation layer on the substrate;

forming a nucleation layer on the first insulation layer;

patterning the nucleation layer to cover the nucleation layer such that portions of the nucleation layer remain exposed;

forming nanotubes on the exposed portions of the nucleation layer, the nanotubes oriented to be substantially vertical in relation to the substrate;

forming an insulative layer over exterior walls of the nanotubes;

forming rings of conductive material about the exterior walls of the nanotubes; and

forming a second insulation layer over the exterior walls of the nanotube.

22. A method of making an electrical interconnect in a semiconductor device comprising:

providing a substrate having a first trace layer;

forming a nucleation layer on the substrate;

patterning the nucleation layer such that a portion of the nucleation layer remains exposed;

forming a nanotube on the exposed portion of the nucleation layer, the nanotube having a lower end connected to the first trace layer;

forming an oxide layer over exterior walls of the nanotube and over the nucleation layer;

patterning the oxide layer to expose an upper end of the nanotube; and

forming a second trace layer such that the upper end of the nanotube is connected thereto.

23. A semiconductor device comprising:

a transistor including a source, a drain, a gate and a channel;

a capacitor including a source, a gate, and a cell;

a single carbon nanotube connected to the source and drain to form the channel of the transistor and the cell of the capacitor.

24. A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring formed about an insulated exterior section of the nanotube, the second conductive ring electrically connected to the substrate;

a third insulation layer formed on the second conductive ring;

a third conductive ring encircling a second end of the nanotube, the third conductive ring providing electrical connection of the second end of the nanotube to the substrate; and

a fourth insulation layer formed over the third conductive ring.

25. The device of claim 24, wherein the nanotube comprises a carbon nanotube.

26. A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling and physically contacting an exterior wall of a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring encircling a first insulated exterior section of the nanotube, the second conductive ring electrically connected at a first end to the substrate;

a third insulation layer formed on the second conductive ring;

a third conductive ring encircling and physically contacting a second insulated exterior section of the nanotube, the third conductive ring electrically connected at a first end to the substrate;

a fourth insulation layer formed on the third conductive ring;

a fourth conductive ring encircling and physically contacting an exterior wall of a second end of the nanotube, the fourth conductive ring providing electrical connection of the second end of the nanotube to the substrate; and

a fifth insulation layer formed on the fourth conductive ring.

27. The device of claim 26, wherein the nanotube comprises a carbon nanotube.

28. A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling and physically contacting an exterior wall of a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring encircling and physically contacting an insulated exterior section of the nanotube, the second conductive ring electrically connected at a first end to the substrate;

a third insulation layer formed on the second conductive layer; and

a conductive layer on the third insulation layer, the conductive layer forming a capacitor ground cell plate, the ground cell plate electrically connected to the substrate.

29. The device of claim 28, wherein the nanotube comprises a carbon nanotube.